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EXAMINER	
BRIER, JEFFERY A	
ART UNIT	PAPER NUMBER
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 09/353,887	Applicant(s) EDWARDS, STEPHEN W.	
	Examiner Jeffery A. Brier	Art Unit 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12 September 2006 and 04 October 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,4-22 and 24-38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1, 4-22 and 24-38 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 10/04/2006 has been entered.

Response to Arguments

2. Applicant's arguments filed 9/12/2006 have been fully considered but they are not persuasive.

The number of references is questioned by applicant at pages 4-5, however, the number of references does not weigh against the obviousness of the claimed invention. In re Gorman, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991) (Court affirmed a rejection of a detailed claim to a candy sucker shaped like a thumb on a stick based on thirteen prior art references.). MPEP 2145V Rev. 5, August 2006. One of ordinary skill in the art would consider these references because they all are computer graphics references that all use textures. Thus, the references when taken together teach a single texture buffer and a plurality of texture processors. Applicant argues that Kobayashi teaches away from using a singe texture buffer when using a plurality of texture processors, however, Kobayashi is concerned with an unlimited number of texture processors, appellant's Brief at page 6, but does not teach away from using a single texture buffer for a limited number of texture processors because a less complex communication bus and arbiter is needed for a limited number of texture processors. Therefore, applicants 9/12/2006 arguments are not persuasive.

The data packet is questioned by applicant at page 5, however, the rejection stated : However, Tanaka et al clearly discloses that the packet data, which represents the storage location of a texture data/map. (See col 2 line 55-62, col 8 line 26-34). Therefore, applicants 9/12/2006 arguments are not persuasive.

The motivation to link five references is questioned in the last paragraph on page 5, however, the motivation given by the examiner of more rapid processing is a goal of one skilled in the computer graphics field in order to better computer generated images.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lentz (U.S. Pat. No. 5,886,705) in view of Young et al (U.S. Pat. No. 5,831,637) and Tanaka et al (U.S. Pat. No. 5,793,371), and further in view of Saunders et al (U.S. Pat. No. 6,046,747) and further in view of Chimoto (U.S. Pat. No. 5,550,961).

Applicant added to claim 1 "wherein the graphics accelerator is configured to convert the associated texture map to a one dimensional texture map by defining a plurality of data blocks within the texture map and then assigning a sequence number to each of the data blocks; and wherein the consecutive data blocks of the texture map are stored consecutively in memory locations". This is taught by Chimoto because Chimoto divides the two dimensional texture into blocks to convert the two dimensional texture for storage into a linear memory. See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line

67-col 7 line 39, col 7 line 55+. Furthermore applicants specification does not define the size of the block, other than it may have 512 data locations, see specification at page 9 line 1, thus, the claimed block's size is open ended and is met by the size of block used by Chimoto.

Regarding claim 1, Lentz discloses that the claimed feature of a graphics accelerator for processing a graphical image, the graphics accelerator comprising: a single texture buffer (21) for storing texture maps (i.e. "texel") and data relating to the texture maps stored in the texture buffer (21) (See Abstract line 1-2, col 2 line 18-20, col 3 line 24-30, col 8 line 15-31); a plurality of texture processors (13 & 24) that perform texturing operations on the graphical image, the plurality of the texture processors retrieving texture packets from the single texture buffer (See Abstract, Fig 1, Fig 2, col 1 line 5-13); each texture processor (13 & 24) including a fetching engine ["pixel-value calculation";15] (See col 2 line 1-2) that retrieves texture packets, each texture packet being stored in the texture buffer (21) and being associated with a texture map that is different than the texture maps associated with any other texture packet in the texture buffer, each texture packet including data ["texture-memory addresses", which identified by texture address; 24) relating to the location of its associated texture map ["texel"] in the texture buffer (21) and data relating to the dimensional type of that texture packet's associated texture map. (See Fig 1, Fig 7, col 1 line 66-col 2 line 4, col 2 line 43-60, col 3 line 10-14, col 3 line 22-36, col 4 line 14-17, col 4 line 42-54, col 5 line 7-11, col 5 line 22-23, col 8 line 46+)

Lentz does not specifically disclose "the texture buffer", as claimed by Applicant. However, a texture buffer is an obvious embodiment of the notoriously well-known texture memory. According to the computer dictionary ["Microsoft Press Computer Dictionary", Third Edition], buffer is defined as "*a region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations, as between an application's data area and an input/output device*". From its definition of "buffer", it is reasonable to interpret "texture memory" of Lentz into "texture buffer" in recited claim, as both are functionally equivalent. [i.e. storing texture data]

Also, Lentz does not explicitly discloses that performing texture operations by multiple texture processors, wherein the plurality of processors retrieve texture packets from the single texture buffer. However, such limitations are shown in the teaching of Young et al. [i.e. 'employing multiple texture processors (251-254) and doing texture mapping with multiple texture processor (251-254), which connected with texture memory (251a-254a)] (See Fig 1, Fig 2 of Young et al) The motivation would have been to minimize the time required for texture processing. Further, as to the computer dictionary ["Microsoft Press Computer Dictionary", Third Edition], "Multiprocessing/Multiprocessor" is defined as "*mode of operation in which two or more connected and roughly equal processing units each carry out one or more processes. In multiprocessing, each processing unit works on a different set of instructions or on different parts of the same process. The objective is increased speed or computing power, the same as in parallel processing and in the use of special units called coprocessors*". Therefore, it would have been obvious to one skilled in the art to employ plurality of texture processors [i.e.

multiple circuitry of 13 in Fin 1 or Lentz] into the teaching of Lentz, thereby reducing texture-processing time effectively. (See suggestions in col 7 line 25-34 of Lentz)

Further, The combination of Lentz and Young et al do not explicitly disclose that a texture packets identifying the location of a texture map. However, Tanaka et al clearly discloses that the packet data, which represents the storage location of a texture data/map. (See col 2 line 55-62, col 8 line 26-34) It would have been obvious to one skilled in the art to incorporate the teaching of Tanaka et al into the teaching of Lentz and Young et al, in order to retrieve proper texels from texture memory with maximized texel data retrieval speed (Also See col 18 line 6-11 in Tanaka et al), as such improvement is also advantageously desirable in the teaching of Lentz and Young et al for accessing the texture data properly and rapidly with optimized memory organization. (See col 2 line 43-56 in Lentz)

Addtionally, the combination of Lentz, Young et al and Tanaka et al do not specifically disclose that texture packet has data relating to the dimensional type of its texture map. However, in an analogous art (texture mapping), Saunders et al discloses that "the special bind texture call includes a target parameter that <u>defines the dimension of the texture map</u> and an ID number that identifies the display list texture object." (See col 6 line 56-67) It would have been obvious to one skilled in the art to incorporate the teaching of Saunders et al into the teaching of Lentz, Young et al and Tanaka et al, in order to provide efficient way to perform texture mapping process based on dimension

type of texture data, as multi-dimensional texture map are used in current computer graphic systems, (also see the suggestions in col 1 line 51 of Lentz "<u>not necessarily two dimensional</u>") it is necessarily required for indicating dimensional type in texture data, because the ordinary skilled in the art would know that different mathematical equations are required for different dimensional type of texture maps, and the three-dimensional texture mapping process will require large capacity processor and much more time to process comparing to one-dimensional texture mapping process, since 3-D texture mapping have more variable to calculate. Therefore, having the texture data, which indicates its dimensional type, is also advantageously desirable in the combination of Lentz, Young et al and Tanaka et al for operating texture mapping process rapidly with no complicated manner.

Further, the combination of Lentz, Tanaka et al and Saunders et al do not explicitly disclose that the "the graphics accelerator is configured to convert the associated texture map to a one dimensional texture map by defining a plurality of data blocks within the texture map and then assigning a sequence number to each of the data blocks; and wherein the consecutive data blocks of the texture map are stored consecutively in memory locations". However, Chimoto discloses converting the associated texture map to a one dimensional texture map by defining a plurality of data blocks within the texture map and then assigning a sequence number to each of the data blocks. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+). It would have been obvious to one skilled in the art to incorporate the

teaching of Chimoto into the teaching of Lentz, Tanaka et al and Saunders et al, in order to operate high-speed texturing without extensive using of texture memory (See col 2 line 16-21, col 5 line 16-25 in Chimoto), as such improvement is also advantageously desirable in the combination of Lentz, Tanaka et al and Saunders et al for operating texture mapping process rapidly with simple modification of memory organization.

Regarding claim 4, Lentz discloses that the dimensional type of each texture map is one of a one-dimensional texture map, a two-dimensional texture map, and a three-dimensional texture map. (See Fig 7)

Regarding claim 5, Lentz discloses that an input for receiving a texture message indicating that a texture map is to be utilized by the texture processor, the fetching engine responsively retrieving selected texture packets from the single texture buffer in response to receipt of the texture message. (See Fig 1)

Regarding claim 6, Lentz discloses that the texture processor [output-image generator; 13] includes a parsing engine [12] for parsing a fetched texture packet and determining information relating to the texture map associated with the fetched texture packet. (See Fig 1; Also See col 2 line 55-62, col 8 line 26-34 in Tanaka et al)

Regarding claim 7, Lentz discloses that the information relates to the location in the texture buffer [21] of the texture map associated with the fetched texture packet. (See Fig 1; Also See col 2 line 55-62, col 8 line 26-34 in Tanaka et al)

Regarding claim 8, Lentz discloses that the information relates to the number of dimensions of the texture map associated with the fetched texture packet. (See Fig 1; Also See col 2 line 57-60 in Saunders et al)

5. Claims 21-22 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lentz (U.S. Pat. No. 5,886,705) in view of Young et al (U.S. Pat. No. 5,831,637) and Tanaka et al (U.S. Pat. No. 5,793,371), and further in view of Saunders et al (U.S. Pat. No. 6,046,747).

Regarding claim 21, claim 21 is similar in scope to the claim 1 with the exception that the new claim limitation added into claim 1 was not added into this claim, and thus the rejections to claim 1 hereinabove is also applicable to claim 21 with the exception that Chimoto is not needed.

Regarding claim 22, Lentz discloses that texture packet includes data relating to the location of its associated texture map in the single texture buffer. (See Fig 7)

Regarding claims 24-25, claims 24-25 are similar in scope to the claims 5-6, and thus the rejections to claims 5-6 hereinabove are also applicable to claims 24-25.

6. Claims 9-13, 15-19 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lentz (U.S. Pat. No. 5,886,705) in view of Tanaka et al (U.S. Pat. No. 5,793,371), and further in view of Saunders et al (U.S. Pat. No. 6,046,747).

Regarding claim 9, Lentz discloses that the claimed feature of a method of applying texture to a graphical image employing a graphics accelerator with a plurality of texture processors, the method comprising: locating a texture packet ["texel" or "texture address data"] identifying the location of a texture map in a single memory device [21], wherein the texture packet is associated with the texture map that is different than texture maps associated with other texture packets; parsing [12,13] the texture packet to determine the location and the number of dimensions of the texture map; retrieving, based upon the determined location, the texture map from the single memory device [21]; applying the texture map to the graphical image. (See Fig 1, Fig 2, Fig 7, col 1 line 66-col 2 line 4, col 2 line 43-60, col 3 line 10-14, col 3 line 22-36, col 4 line 14-17, col 4 line 42-54, col 5 line 7-11, col 5 line 22-23, col 8 line 46+)

Lentz does not explicitly disclose that a texture packets identifying the location of a texture map. However, Tanaka et al clearly discloses that the packet data, which represents the storage location of a texture data/map. (See col 2 line 55-62, col 8 line

26-34) It would have been obvious to one skilled in the art to incorporate the teaching of Tanaka et al into the teaching of Lentz, in order to retrieve proper texels from texture memory with maximized texel data retrieval speed (Also See col 18 line 6-11 in Tanaka et al), as such improvement is also advantageously desirable in the teaching of Lentz and Young et al for accessing the texture data properly and rapidly with optimized memory organization. (See col 2 line 43-56 in Lentz)

Finally, The combination of Lentz, Young et al and Tanaka et al do not specifically disclose that texture packet has data relating to the dimensional type of its texture map. However, in an analogous art (texture mapping), Saunders et al discloses that "the special bind texture call includes a target parameter that defines the dimension of the texture map and an ID number that identifies the display list texture object." (See col 6 line 56-67) It would have been obvious to one skilled in the art to incorporate the teaching of Saunders et al into the teaching of Lentz, Young et al and Tanaka et al, in order to provide efficient way to perform texture mapping process based on dimension type of texture data, as multi-dimensional texture map are used in current computer graphic systems, (also see the suggestions in col 1 line 51 of Lentz "not necessarily two dimensional") it is necessarily required for indicating dimensional type in texture data, because the ordinary skilled in the art would know that different mathematical equations are required for different dimensional type of texture maps, and the three-dimensional texture mapping process will require large capacity processor and much more time to process comparing to one-dimensional texture mapping process, since 3-D texture

mapping have more variable to calculate. Therefore, having the texture data, which indicates its dimensional type, is also advantageously desirable in the combination of Lentz, Young et al and Tanaka et al for operating texture mapping process rapidly with no complicated manner.

Regarding claim 10, Lentz discloses that the texture packet is located by accessing a record identifying the location of the texture packet. (See Abstract, Fig 1, Fig 7, col 2 line 48-60, col 4 line 14-17, col 4 line 42-54, col 5 line 7-11, col 8 line 15-31)

Regarding claim 11, Lentz discloses that the single memory device is texture memory. (See Fig 1)

Regarding claim 12, Lentz discloses that the texture packet is stored in the single memory device. (See Fig 1)

Regarding claim 13, Lentz discloses that reconstructing the texture map after it is retrieved from the single memory device. (See Fig 1, Fig 7)

Regarding claims 15-19, claims 15-19 are similar in scope to the claims 9-13, and thus the rejections to claims 9-13 hereinabove are also applicable to claims 15-19.

Regarding claim 35, Lentz discloses that the claimed feature of a data structure for storing data relating to a texture map ["texel"], the texture map having an associated dimension and being stored at a given location ["address"] in a single memory device, the apparatus comprising: a location field [i.e. "address"] identifying the given location in the memory device; a dimension field identifying the dimension of the texture map (See Fig 1, Fig 7)

Lentz does not explicitly disclose that a texture packets identifying the location of a texture map. However, Tanaka et al clearly discloses that the packet data, which represents the storage location of a texture data/map. (See col 2 line 55-62, col 8 line 26-34) It would have been obvious to one skilled in the art to incorporate the teaching of Tanaka et al into the teaching of Lentz (Also See col 18 line 6-11 in Tanaka et al), in order to retrieve proper texels from texture memory with maximized texel data retrieval speed, as such improvement is also advantageously desirable in the teaching of Lentz and Young et al for accessing the texture data properly and rapidly with optimized memory organization. (See col 2 line 43-56 in Lentz)

Also, The combination of Lentz, Young et al and Tanaka et al do not specifically disclose that texture packet has data relating to the dimensional type of its texture map. However, in an analogous art (texture mapping), Saunders et al discloses that "the special bind texture call includes a target parameter that <u>defines the dimension of the texture map</u> and an ID number that identifies the display list texture object." (See col 6

line 56-67) It would have been obvious to one skilled in the art to incorporate the teaching of Saunders et al into the teaching of Lentz, Young et al and Tanaka et al, in order to provide efficient way to perform texture mapping process based on dimension type of texture data, as multi-dimensional texture map are used in current computer graphic systems, (also see the suggestions in col 1 line 51 of Lentz "not necessarily two dimensional") it is necessarily required for indicating dimensional type in texture data, because the ordinary skilled in the art would know that different mathematical equations are required for different dimensional type of texture maps, and the three-dimensional texture mapping process will require large capacity processor and much more time to process comparing to one-dimensional texture mapping process, since 3-D texture mapping have more variable to calculate. Therefore, having the texture data, which indicates its dimensional type, is also advantageously desirable in the combination of Lentz, Young et al and Tanaka et al for operating texture mapping process rapidly with no complicated manner.

Regarding claim 36, Lentz discloses that the texture map comprises a set of mipmaps, further wherein the location field includes a plurality of subfields, each subfield identifying the location of one mipmap in the set of mipmaps. (See Fig 1, Fig 2, Fig 7, col 1 line 66-col 2 line 4, col 2 line 43-60, col 3 line 10-14, col 3 line 22-36, col 4 line 14-17, col 4 line 42-54, col 5 line 7-11, col 5 line 22-23, col 8 line 46+)

Regarding claim 37, Lentz discloses that the texture map spans a plurality of addresses in the memory device, the location field identifying the plurality of addresses. (See Fig 1, Fig 7)

Regarding claim 38, Lentz discloses that the data structure is stored in the memory device, the memory device being texture memory. (See Fig 1)

7. Claims 14, 20, 26-28 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lentz (U.S. Pat. No. 5,886,705) and Tanaka et al (U.S. Pat. No. 5,793,371) in view of Saunders et al (U.S. Pat. No. 6,046,747), and further in view of Chimoto (U.S. Pat. No. 5,550,961).

Regarding claim 14, the combination of Lentz, Tanaka et al and Saunders et al fails to explicitly disclose that the texture map being reconstructed based upon the determined dimensional type of the texture map. However, Chimoto discloses that reconstructing the two-dimensional texture data as one-dimensional texture data. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+) It would have been obvious to one skilled in the art to incorporate the teaching of Chimoto into the teaching of Lentz, Tanaka et al and Saunders et al, in order to operate high-speed texturing without extensive using of texture memory (See col 2 line 16-21, col 5 line 16-25 in Chimoto), as such improvement is also advantageously desirable in the

teaching of Lentz for operating texture mapping process rapidly with simple modification of memory organization.

Regarding claim 20, claim 20 is similar in scope to the claim 14, and thus the rejection to claim 14 hereinabove is also applicable to claim 20.

Regarding claim 26, as similar to claim 1 hereinabove, Lentz discloses that the claimed feature of a method of storing a texture map in linear texture memory of a graphics accelerator, the method comprising: a) determining the dimension of the texture map ["texel"]; b) converting the texture map to a one dimensional texture map if the dimension of the texture map is determined to be more than one dimensional, the one dimensional texture map having a first number of consecutive data blocks; c) locating a second number of consecutive memory locations in the texture memory, the first number being equal to the second number; d) storing the one dimensional texture map in the located memory locations in the texture memory. (See Fig 1, Fig 7, col 1 line 66-col 2 line 4, col 2 line 43-60, col 3 line 10-14, col 3 line 22-36, col 4 line 14-17, col 4 line 42-54, col 5 line 7-11, col 5 line 22-23, col 8 line 46+)

Lentz does not explicitly disclose that a texture packets identifying the location of a texture map. However, Tanaka et al clearly discloses that the packet data, which represents the storage location of a texture data/map. (See col 2 line 55-62, col 8 line 26-34) It would have been obvious to one skilled in the art to incorporate the teaching

of Tanaka et al into the teaching of Lentz, in order to retrieve proper texels from texture memory with maximized texel data retrieval speed (Also See col 18 line 6-11 in Tanaka et al), as such improvement is also advantageously desirable in the teaching of Lentz and Young et al for accessing the texture data properly and rapidly with optimized memory organization. (See col 2 line 43-56 in Lentz)

Also, The combination of Lentz, Young et al and Tanaka et al do not specifically disclose that texture packet has data relating to the dimensional type of its texture map. However, in an analogous art (texture mapping), Saunders et al discloses that "the special bind texture call includes a target parameter that defines the dimension of the texture map and an ID number that identifies the display list texture object." (See col 6 line 56-67) It would have been obvious to one skilled in the art to incorporate the teaching of Saunders et al into the teaching of Lentz, Young et al and Tanaka et al, in order to provide efficient way to perform texture mapping process based on dimension type of texture data, as multi-dimensional texture map are used in current computer graphic systems, (also see the suggestions in col 1 line 51 of Lentz "not necessarily two dimensional") it is necessarily required for indicating dimensional type in texture data, because the ordinary skilled in the art would know that different mathematical equations are required for different dimensional type of texture maps, and the three-dimensional texture mapping process will require large capacity processor and much more time to process comparing to one-dimensional texture mapping process, since 3-D texture mapping have more variable to calculate. Therefore, having the texture data, which

indicates its dimensional type, is also advantageously desirable in the combination of Lentz, Young et al and Tanaka et al for operating texture mapping process rapidly with no complicated manner.

Further, the combination of Lentz, Tanaka et al and Saunders et al do not explicitly disclose that the texture map being reconstructed based upon the determined dimensional type of the texture map. However, Chimoto discloses that reconstructing the two-dimensional texture data as one-dimensional texture data. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+) It would have been obvious to one skilled in the art to incorporate the teaching of Chimoto into the teaching of Lentz, Tanaka et al and Saunders et al, in order to operate high-speed texturing without extensive using of texture memory (See col 2 line 16-21, col 5 line 16-25 in Chimoto), as such improvement is also advantageously desirable in the combination of Lentz, Tanaka et al and Saunders et al for operating texture mapping process rapidly with simple modification of memory organization.

Regarding claim 27, refer to the discussion for the claim 26 hereinabove, Chimoto further discloses that step b) comprising: B1) defining a plurality of data blocks within the texture map (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+) B2) assigning a sequence number to each of the data blocks, the sequence numbers being consecutive numbers. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+)

Regarding claim 28, refer to the discussion for the claim 26 hereinabove, Chimoto discloses that step d) comprising: D1) consecutively storing each consecutive data block of the one dimensional texture map in the located memory locations. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+)

Regarding claims 32-34, claims 32-34 are similar in scope to the claims 26-28, and thus the rejections to claims 26-28 hereinabove are also applicable to claims 32-34.

8. Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lentz (U.S. Pat. No. 5,886,705), Tanaka et al (U.S. Pat. No. 5,793,371) and Saunders et al (U.S. Pat. No. 6,046,747) in view of Chimoto (U.S. Pat. No. 5,550,961), and further in view of Young et al (U.S. Pat. No. 5,831,637).

Regarding claim 29, claim 29 is similar in scope to the claim 26, and thus the rejection to claim 26 hereinabove is also applicable to claim 29. In addition, Lentz does not specifically discloses a plurality of texture processors. However, such limitations are shown in the teaching of Young et al. [i.e. 'employing multiple texture processors (251-254) and doing texture mapping with multiple texture processor (251-254), which connected with texture memory (251a-254a)] (See Fig 1, Fig 2 of Young et al) The motivation would have been to minimize the time required for texture processing. Further, as to the computer dictionary ["Microsoft Press Computer Dictionary", Third Edition], "Multiprocessing/Multiprocessor" is defined as "*mode of operation in which two or*

more connected and roughly equal processing units each carry out one or more processes. In multiprocessing, each processing unit works on a different set of instructions or on different parts of the same process. The objective is increased speed or computing power, the same as in parallel processing and in the use of special units called coprocessors". Therefore, it would have been obvious to one skilled in the art to employ plurality of texture processors [i.e. multiple circuitry of 13 in Fin 1 or Lentz] into the combination of Lentz, Tanaka et al, Saunders et al and Chimoto, thereby reducing texture-processing time effectively. (See suggestions in col 7 line 25-34 of Lentz)

Regarding claims 30-31, claims 30-31 are similar in scope to the claims 27-28, and thus the rejections to claims 27-28 hereinabove are also applicable to claims 30-31.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffery A Brier whose telephone number is (571) 272-7656. The examiner can normally be reached on M-F from 7:00 to 3:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi, can be reached at (571) 272-7664. The fax phone Number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffery A. Brier

Jeffery A Brier
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